**International Journal of Advanced Research and Development**
**ISSN: 2455-4030**
**Impact Factor: RJIF 5.24**
**www.advancedjournal.com**
**Volume 3; Issue 2; March 2018; Page No. 318-321**

# SRR design issues for wireless communication

**Dr. Bharat Naresh Bansal**
MIMIT, Malout, Punjab, India

**Abstract**
The term Software radio receiver (SRR) comes in the class of re-programmable or reconfigurable radios which was introduced by Joe Mitola. SRR or Software defined Radio (SDR) is a radio that offered flexibility by using software with the static hardware. Hence, the same piece of hardware can be used to carry out different tasks at different time. This paper highlights the essential steps required for the development of SRR design for communication system. Performance of SRR can be best examined by proper selection of the different components used in SRR.

**Keywords:** SRR, SDR, ADC, filter etc.

## 1. Introduction
The wireless industries are growing exponentially with the development of multifunctional, multi-mode communication standards and new radio access technologies. SDR. Technology is predicted to replace many of the conventional methods to implement transmitter and receiver, which offers extensive advantages that includes adaptability, multifunctionality and reconfigurability encompassing radio frequency bands, waveforms, modes of operation and air interface.

### 1.1 Software Radio Receiver (SRR)
The receiver which is used in SDR is known as SDR receiver or SRR. SRR requires real time variable frequency response characteristics, which are defined by software. In SRR, Channelizer is the most intensive computational part, which operates at high sampling rate. The process of extracting multiple narrowband radio channels from a wideband input signal in SRR is known as channelization. The filters that are used for channelization are called channel filters. Channel filter used in SRRs should have low complexity and reconfigurability property. The bandwidth of the filter is the important characteristic in radio receiver that selects the desired channel. Desired channel is selected using sharp filters having different bandwidths in SRR. The large number of filter coefficients and different computational resources are its major requirements. So, SDR receiver or SRR can receive channels of wide range of bandwidth and any modulation.
Figure 1.3 shows the basic block diagram of SRR. The receiver starts with smart antenna which is used to minimize different type of noise, multipath and interference by providing gain versus direction characteristic. Similar advantages are also provided by the smart antenna to the transmitter.

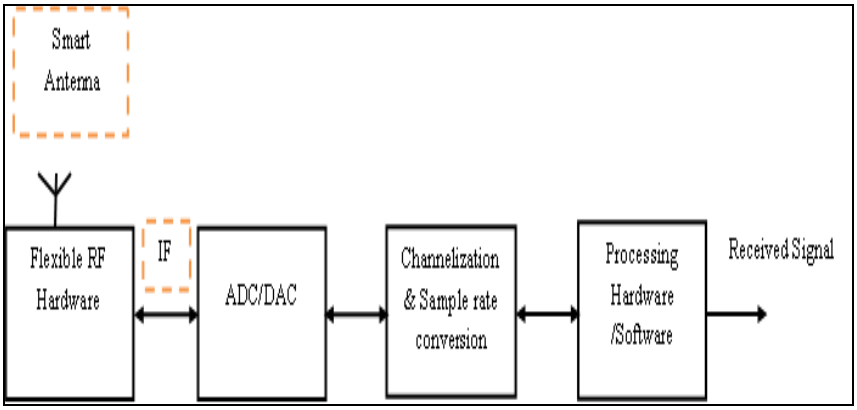


**Fig 1:** Basic block diagram of SRR

In conventional SRR, low noise amplifier (LNA) is used for amplifying and filtering the radio frequency (RF) signal received by antenna, which after mixing with local oscillator (LO) produces an Intermediate frequency (IF). The IF range signal is digitized using analog to digital converter (ADC) eliminates imaging and carrier offset problems. Digital to analog converter (DAC) is used to convert digital to analog signal for transmitter. In the next stage, digital filtering is used for channelization process. Interfacing between the output of ADC and processing hardware is achieved using sample rate

conversion. Different types of platforms are used for software processing like DSPs, Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs). The different type of software methods have been used for modulation and demodulation of the signal such as middleware or virtual radio machines.

### 1.2 Applications of SRR

Following are the applications of SRR:

a. In military as the Joint Tactical Radio System.
b. SRR is equally useful for commercial purposes, as commercial sector defines SRR as one that implements a specified range of capabilities through elements which are software reconfigurable.
c. It is securely upgradable which can be used in internet as medium for updates.

## 2. Software Radio Receiver (SRR) or Software define Radio (SDR)

Zangi and Koilpillai (1998) [2] presented an algorithm for implementing computationally efficient FB channelizer to extract individual channels from the output of the wideband ADC. The input to the IF processing block is output of the ADC in SRR. The IF processing block in SRR implemented by using the computationally efficient algorithm. In this algorithm instead of classical DFTFB channelizer a subsampled DFTFB channelizer was used. The complexity of the implemented channelizer was significantly less than the complexity of the traditional channelizers. Fixed channel stacking is major drawback of DFTFBs.

Seskar and Mandayam (1999) [3] presented a reconfigurable architecture for linear multiuser detection. SRR was implemented to achieve dynamic reconfiguration. Authors have divided the functionality of the architecture into two parts according to processing speed requirements that is FPGA and DSP. The architecture provided diverse Quality of Service (QoS) guarantees ranging in several orders of magnitudes in terms of Bit Error Rate (BER) requirements. The architecture was flexible, therefore it allows a different signal processing approaches for implementation of required estimation. Moreover, the experimental results showed that diverse services such as voice and data traffic were simultaneously supported using this architecture. There was degradation in receiver performance due to fixed point arithmetic, which was compensated by 4-bit quantization.

Zangi and Koilpillai (1999) [4] described two key issues in the design of wideband SRR which are: a) a single ADC used to digitize a large block of the cellular spectrum, and b) efficient channelizers used to extract individual channels from the wide-band signal. Authors also presented a new computationally efficient wide-band channelizer known as opened filter bank (OFB) channelizer, which was closely related to the DFT filter bank used in transmultiplexers. The complexity of the OFB channelizer was less than the complexity of the canonical DFT filter.

Yoshida, Otaka, Kato and Tsurumi (2000) [5] developed a SDR using direct conversion principle. An analog quadrature demodulator with fixed frequency local oscillator prepared for each band and was used to down convert entire channel bandwidth to baseband. The two characteristics were required for analog stage to down convert the entire bandwidth of various communication equipments with different frequency band to the baseband, which are: a) Multi-band characteristic and b) Broadband characteristic. The developed SDR receiver was realized multiband characteristics at 1.5 GHz and 1.9 GHz band and broadband characteristic up to 10 MHz together with demodulation function of quadrature phase shift keying (QPSK) and gaussian minimum shift keying (GMSK). Improvement in design could be achieved by balancing the quadrature demodulator in order to increase the image cancel ratio.

Harris and Rice (2001) [8] proposed poly phase filter banks for symbol timing synchronization in SDR. The poly phase filter bank have separated interpolation and matched filters. No interpolation filter required after the matched filter and provided a natural way to incorporate maximum likelihood timing estimation into the loop. Moreover, the samples produced were aligned in both phase and frequency with the data clock. Authors have also proved the equivalency of polyphase indexing to the fractional interpolation interval. The approach has high phase noise which did not allow the ADC to be placed at the IF.

Xu, Wu and Bosisio (2003) [6] designed a SDR architecture using Six Port technology or multi-port demodulator to provide multimode and multi-channel wireless receiver. Six-port was consisted by interconnecting combiners and dividers in such a way that the signal which has to be measured along with four different sums of reference signal was produced. The results of the actual integrated SDR and Six-Port technology circuit provided low cost system, large flexibility in system design, and also huge potential for software reuse.

Schnepp, Muller, Luy and Russer (2003) [7] implemented channel diversity for mobile SRR. It overcomes the received signal distortion due to multipath fading. The technique was based on Software Radio architecture, so the technique was easily extended to more communication channels. A coherent superposition of multiple information from several transmitters at different frequencies to increase the reception quality was implemented in this technique. Moreover, presented technique was an alternative to antenna diversity, which resulted in a reduction of the number of antennas. However, there was fading effect in the superposed signal due to doppler frequencies from different transmitter.

Yeung and Chan (2004) [8] presented multiplier-less realization and design of SRR with reduced system delay. Authors studied two approaches; a) multiplier-less hardware realization), and b) realize the SRR using DSP. The fixed coefficients of SRR were efficiently implemented with fewer numbers of additions and shifts using the SOPOT representations. The design was implemented by applying digital all pass filters and low delay FIR filters to significantly reduce the system delay of the multistage decimators in SRRs. Sampling Rate Converter (SRC) was used to avoid the need of costly programmable FIR filter in the conventional SRR. This SRC was implemented using a variable digital filter immediately after the integer decimators. Hence, the design has reduced system delay and implementation complexities.

Xu, Bosisio and Wu (2005) [9] presented a SRR platform based on Substrate Integrated Waveguide (SIW) six-port structure. The structure was compact and has lower cost. It

does not require any external terminal as conventional six port structure. The operating frequency of receiver was from 22GHz to 26GHz for different modulations. The simulation results proved that the platform based on six-port technology was flexible and stable in system configuration, which could be used in software defined radio applications.

Araujo and Dinis (2007) [10] presented an analytical approach to evaluate quantization effects in ADC which used in SRR design. Authors taken benefit of the Gaussian behavior of the multiband/multiuser signal at the input of a wideband ADC and was used for optimization of quantization characteristic in a simple and computationally efficient way and the performance evaluation. An improvement in SIR level of several decibels was achieved by using oversampling factor and reference frequency.

Harju and Nurmi (2007) [11] worked on a programmable hardware platform to implement the WCDMA and orthogonal frequency division multiplexing (OFDM) baseband SRR. The design consisted of three coprocessors and Reduce Instruction Set Computer (RISC) core, which were used to execute the computation kernels of the receiver algorithms. Low level programming did not require in the programming part of the presented design. C based test bench was used in the system to simulate the design and the simulation results showed that design and the programming interface provided resources to implement OFDM and WCDMA baseband SRR. Practical implementation of the design showed that the power consumption and area required in this were less. The power consumption of the entire platform was not estimated due to practical limitations of the simulation environment.

Awan, Alam, Koch and Behjou (2007) [12] presented design and implementation of Multi Standard SRR based on FPGA. RF signal after LNA was directly sampled at 840 MHz by bandpass sampling technique. Moreover, the front end processed different signal in the digital domain, which removed the hardware limitations as presented by conventional design. Polyphase channelizers were used for extracting channels of 12 Universal Mobile Telecommunications System (UMTS) and 3 Wireless Local Area Network (WLAN) with desired rate at the baseband. The design was implemented using different structural techniques. Serial Polyphase filter structure with parallel Multiplier and Accumulator (MAC) was used for given design. By critically analyzing the design in terms of hardware, it is proved that the Distributed Arithmetic or Xilinx DSP48 blocks were efficient and best for implementing the polyphase channelizer. However, there was need of various standard polyphase channelizers to extract all the channels.

Mirzaei, Chehrazi, Bagheri and Abidi (2009) [13] synthesized and designed a second order filter for a SRR. The designed filter provided a wider and deeper attenuation to aliasing blockers prior to sampling. Designed filter was superior to first order filter due to its advantages: a) Exclusion of decimation stages, b) Initial rate of sampling was lower, c) Simple clocking scheme. Authors also studied various imperfections like gain mismatch, transconductor output impedance, and residual offsets in the channels by analyzing the noise and linearity performance of the filter. Moreover, it was observed that the filter was robust to clock jitter and suited for flicker noise cancellation. It offered comparable power consumption in spite of six transconductors.

Mahesh and Vinod (2011) [14] introduced a computational efficient, flexible and reconfigurable FBs for non-uniform as well as uniform channelization in SRR using coefficient decimation. Their FB were capable to receive channels of multiple communication standards at same time, whereas opposite to this DFTFB based receiver required separate FBs for simultaneous reception of multiple communication standard channels. The proposed method was focused on SRR application and was employed to all scenarios where DFTFB was used. In this paper emphasis should be given on energy consumption by the SRR.

Cruz, and Carvalho (2011) [15] presented an enhanced architecture to increase the dynamic range of ADC in a SRR without using more number of components and flexibility. The design increased the dynamic range of ADC which was equal to value of the attenuator used. Moreover, the flexibility property of the design allowed it to use in band pass sampling and variety of receivers without increasing the complexity of front end. The design was used for wide band receiver in SDR. However, it consumed more DC power and nonlinear distortion because it was based on active devices. Moreover, the design showed improvements in performance, when simulations with two different modulated signals were performed. The results showed that with this design 10 dB increase in the dynamic range was achieved which was controlled by the attenuator. Complexity of the model could be optimized by the tradeoff between number of devices and outcome.

Ben-Romdhane, Rebai, Ghazel, Desgreys, and Loumeau (2011) [16] presented a non-uniformly controlled ADC for multistandard SRR by defining the numerical constraint related to the random sampling frequency. The design in the baseband stage attempted to share as much hardware as possible. Further, the Automatic gain control (AGC) block was avoided in the designed baseband stage, which relaxed the nonprogrammable anti-aliasing filter from fourth to third order. A relaxed design was employed for an E-GSM/UMTS/IEEE802.11 multistandard receiver. Baseband stage saves 40% of power consumption and further10% of power consumption over the total power of the receiver.

Deng, Huang, Liu, Li, Huang, and Yi (2013) [17] designed and implemented both ADC and Digital down Converter (DDC) in system on chip for IF digital SRR. Transformation of an IF analog signal to baseband digital signal was done. Hence, the design made the SRR system more flexible, higher integrated and more reliable as compared to the combination functions of FPGA and DSP. Further, SoC was capable of accepting data at a 200MHz sample rate. The simulation results showed that the design worked well for different types of wireless applications.

## 3. Conclusion

So, the basic idea of SDR is to provide flexibility to communication system through the property of reconfigurability by substituting the analog signal processing with digital signal processing. So, for implementing SDR architecture both flexibility and low complexity are required for filter. SDR can considerably reduce the complexity and cost of base stations for wireless communication system. In

SDR wideband ADC and DAC are used as close to antenna as possible. Digital domain is used for all signal processing and functionality. The power consumption in SRR can be minimized by altering the filter coefficients.

## 4. References


1. Mitola J. III Software Radios-Survey, Critical Evaluation and Future Directions, IEEE National Telesystems Conference, Washington, DC, 1992, 15-23.
2. Zangi KC, Koilpillai RD. Efficient Filterbank Channelizers for Software Radio Receivers, IEEE International Conference on Acoustics, Speech and Signal Processing, Seattle, WA. 1998; 6:3497-3500.
3. Seskar IP, Mandayam NB. A Software Radio Architecture for Linear Multiuser Detection, Journal on Selected Areas in Communications. 1999; 17(5):814-823.
4. Zangi KC, Koilpillai RD. Software Radio Issues in Cellular Base Stations, IEEE Journal on Selected Areas in Communications. 1999; 17(4):561-573.
5. Yoshida H, Otaka S, Kato T, Tsurumi H. A Software Defined Radio Receiver using the Direct Conversion Principle: Implementation and Evaluation, IEEE International Symposium on Personal, Indoor and Mobile Radio Communications, London. 2000; 2:1044-1048.
6. Harris FJ, Rice M. Multirate Digital Filters for Symbol Timing Synchronization in Software Defined Radios, Journal on Selected Areas in Communications. 2000; 19(12):2346-2357.
7. Xu X, Wu K, Bosisio RG. Software Defined Radio Receiver Based on Six-Port Technology, IEEE MTT-S International Microwave Symposium Digest, Philadelphia, USA. 2003; 2:1059-1062.
8. Schnepp H, Muller T, Luy JF, Russer P. The Implementation of Channel Diversity in Mobile Software Radio Receivers, IEEE Microwave and Wireless Components Letters. 2003; 13(8):323-325.
9. Yeung KS, Chan SC. The Design and Multiplier-less Realization of Software Radio Receivers with Reduced System Delay, IEEE Transactions on Circuits and Systems-I: Regular Papers. 2004; 51(12):2444-2459.
10. Xu XR, Bosisio G, Ke W. Analysis and Implementation of Software Defined Radio Receiver Platform, Asia-Pacific Microwave Conference Proceedings, 2005, 5.
11. Araujo T, Dinis R. Analytical Evaluation and Optimization of the Analog-to-Digital Converter in Software Radio Architectures, IEEE Transactions on Vehicular Technology. 2007; 56(4):1964-1970.
12. Harju L, Nurmi J. Hardware platform for Software Defined WCDMA/OFDM Baseband Receiver Implementation, IET Computers and Digital Techniques. 2007; 1(5):640-652.
13. Awan MUR, Alam MM, Koch P, Behjou N. Design and Implementation of an FPGA-based Multi-standard Software Radio Receiver, Norchip Conference, Aalborg, 2007, 1-5.
14. Mirzaei A, Chehrazi S, Bagheri R, Abidi AA. A Second-Order Antialiasing Prefilter for a Software-Defined Radio Receiver, IEEE Transactions on Circuits and Systems-I: Regular Papers. 2009; 56(7):1513-1524.
15. Cruz PM, Carvalho NB. Enhanced Architecture to increase the Dynamic range of SDR Receivers", IEEE Radio and Wireless Symposium, Phoenix, AZ, 2011, 331-334.
16. Ben-Romdhane M, Rebai C, Ghazel A, Desgreys P, Loumeau P. Nonuniformly Controlled Analog-to-Digital Converter for SDR Multistandard Radio Receiver, IEEE Transactions on Circuits and Systems-II: Express Briefs. 2011; 58(12):862-866.
17. Deng J, Huang X, Liu L, Li Y, Huang X, Tao Y. Design and Implementation of a Mixed SoC for IF Digital Software Radio Receiver, Sixth International Conference on Advanced Computational Intelligence, Hangzhou, China, 2013, 262-265.