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Design of low area static CMOS parallel self-timed adder with low power consumption using conditional approach

[1] G Siva Sai Narayana, [2] KV Ganesh

[1] PG Student, Dept of ECE, VITAM College, Visakhapatnam, Andhra Pradesh, India
[2] Asst. Professor, Dept of ECE, VITAM College, Visakhapatnam, Andhra Pradesh, India

Abstract
Adder is an important circuit used in arithmetic and logic unit and many other applications. There are different types of algorithms used in adders to achieve better performance, low Area and low Power. The main objective of this paper is to provide new low power, area efficient solution for very large scale integration (VLSI) Circuit designers. We have many logic styles such as Swing Restored complementary Pass-transistor Logic (SR-CPL) and Dual Pass-Transistor (DPL), dynamic logic and static logic. Adder has been designed by using Static CMOS logic and it has the disadvantage of more Transistor count. We will also ensure that speed will not be worse by making sure that not more than four number of transistors are in series either in pull-up or pull-down network of CMOS. Cells which were being used has limited fan-in as well as fan-out, though asynchronous logic is employed. The proposed Adder has been designed and simulated by using TANNER EDA Tool.

Keywords: static CMOS, conditional approach, XOR, MUX

Introduction
Adder used Transmission gates which does not have Power rails, Static CMOS which has only Disadvantage of more number of Transistors and Pseudo NMOS logic which has charge sharing problems [1]. Wave pipelining is a method to increase the Performance of the system and Clock period of such a system is difference of Maximum and Minimum delay [1]. Carry signals are organized in a Tree manner [2] but not in a Chain fashion which degrades the Speed Asynchronous systems has more performance and low Power but they are difficult to design and computation will be done only when necessary [3]. CMOS has reliable operation as well as high noise margins even though the Voltage is scaled which means logic levels will be degraded and it also supports minimum number of Transistor sizes [4]. Multi threshold CMOS technologies has circuits with uneven threshold voltages like more is the threshold voltage more is the delay so reduction in threshold voltages will be done for Transistors which are involved in the Critical path so that Critical path performance can be enhanced [5]. Adder has been designed in many logic styles to analyze the results but still 28T Full Adder is the Designer choice in most cases as it is designed in Static CMOS, though it supports limited Fan-out it can be made better by introducing Buffers [6]. Adder has been designed in pass transistor logic which has problem of Logic level degradation and it also has non-uniform structure [7]. There is a recommendation that not more than four number of Transistors should be there in series either in pull-up or pull-down region [8]. Asynchronous Adders are based on full dual rail encoding of all the signals and these are difficult to design when in compared with Synchronous circuts [9].

2. Conditional Approach
In this paper we introduce a new kind of method called conditional approach as follows, When there are 2 inputs and in which if one input is High and other input is Low, it is clear that 2 Demarcation lines are needed because High corresponds to NMOS and Low corresponds to PMOS but whether NMOS to be placed in the First Demarcation line and PMOS to be placed in the Second Demarcation line or Vice versa depends on Output Low(High) requirement and it will be in the form of NMOS – PMOS if Output required is High because through PMOS we will get '1', in the form of PMOS – NMOS if Output required is Low because through NMOS we will get '0', and from First Demarcation line we can get either '0' or '1' so 1 extra PMOS and NMOS for this purpose and anyhow if First Demarcation line has NMOS there will be PMOS and same is the case with Second Demarcation line. Let us see the assumed condition for Output (high) step by step procedure

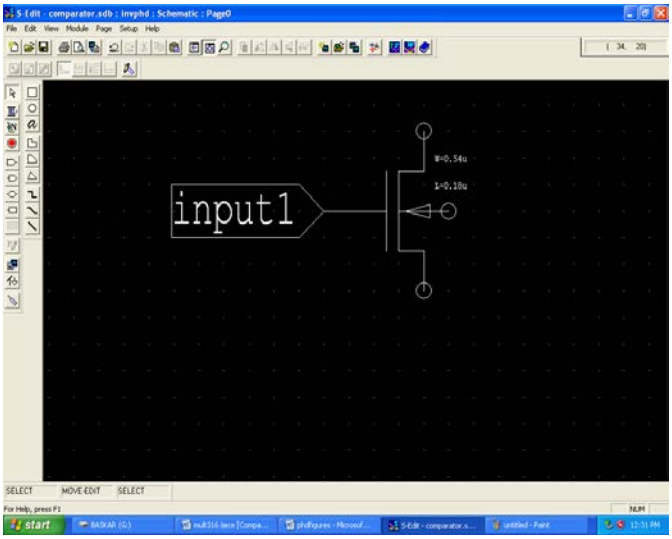

Fig 1: Step 1 input for nmos

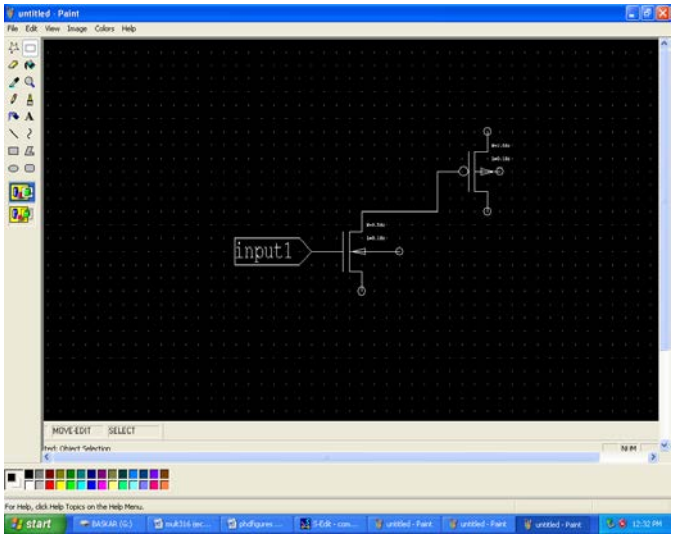

Fig 2: Step 2 connection to input 1

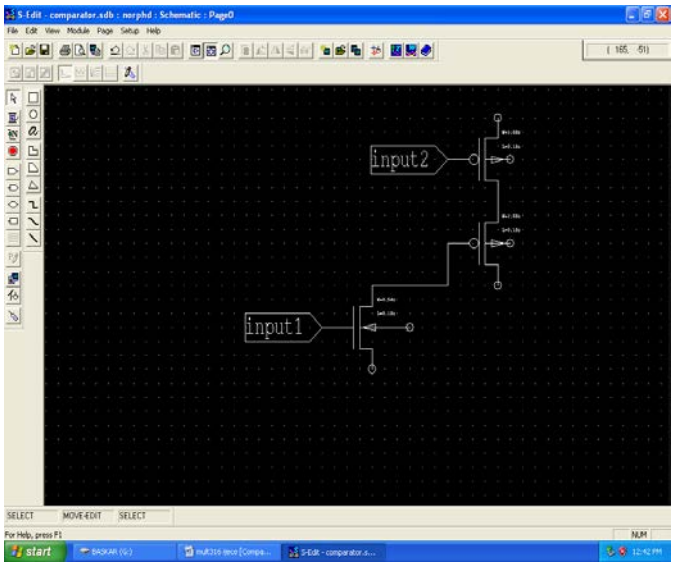

Fig 3: Step 3 connection to input 2

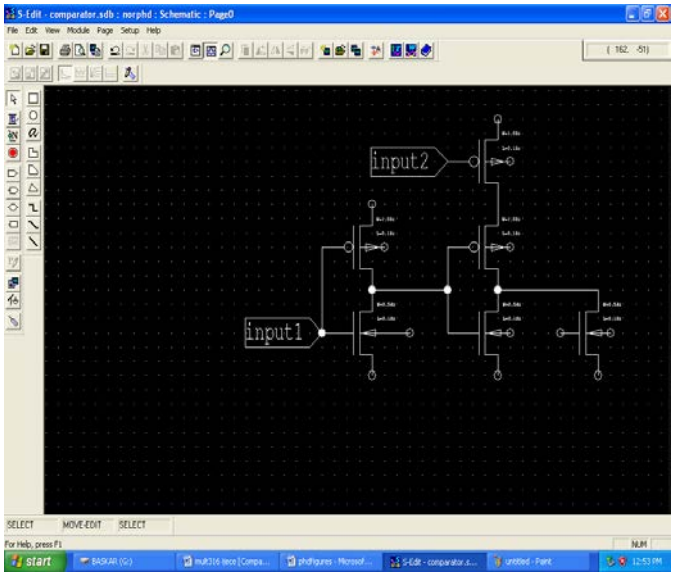

Fig 4: Step 4 to obtain high output

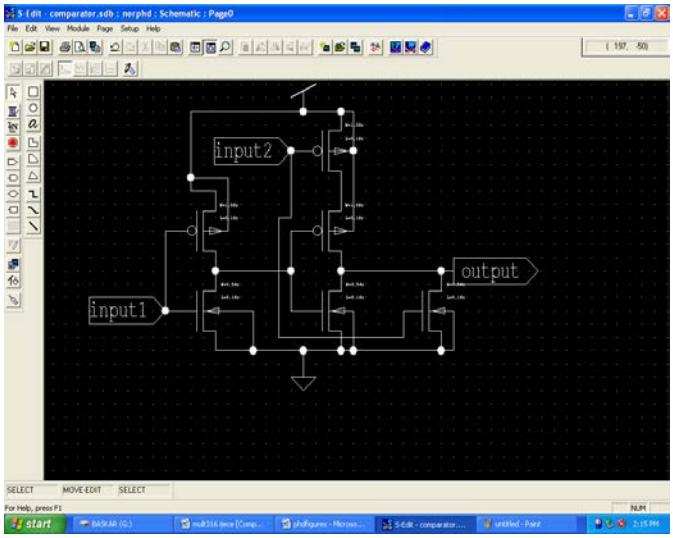

Fig 5: Step 5.complete circuit

Applying the conditions for Output (Low) as followed by steps

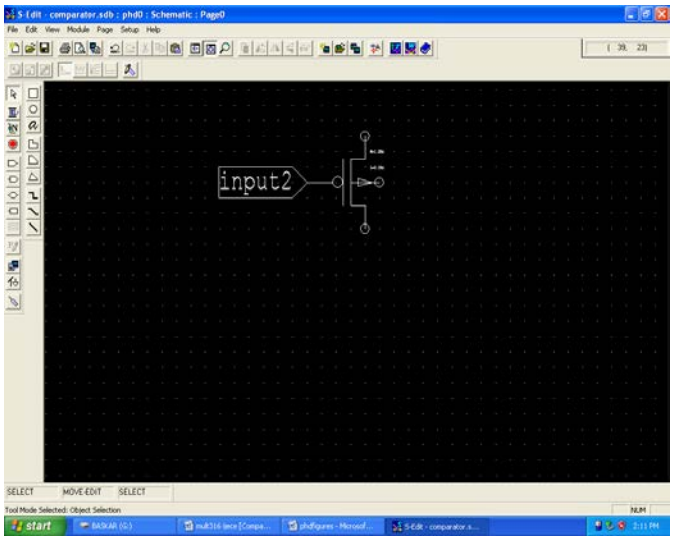

Fig 6: Step 1 input for pmos

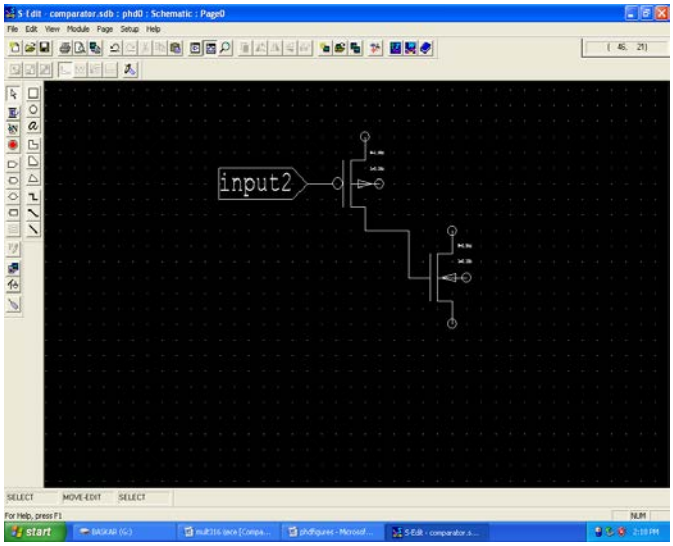

Fig 7: Step 2 connection to input 2

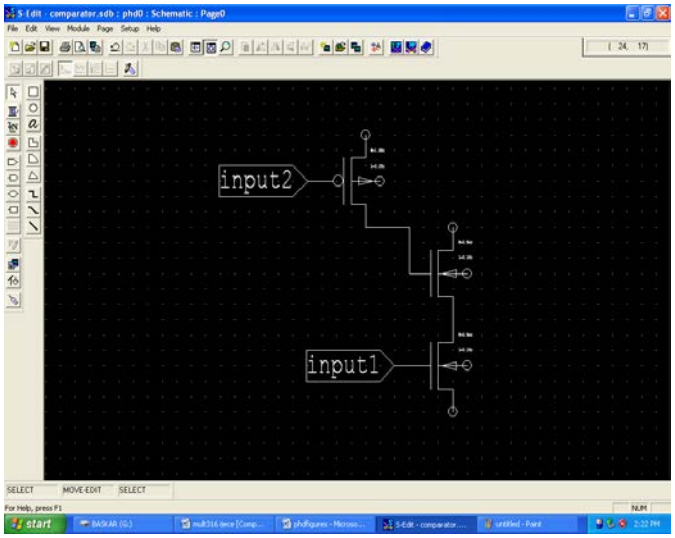

Fig 8: Step 3 connection to input 1.

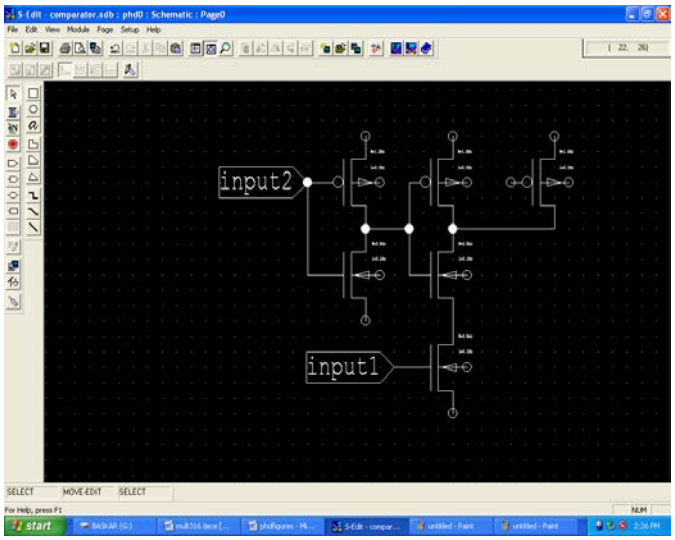

Fig 9: Step 4 to obtain low output.

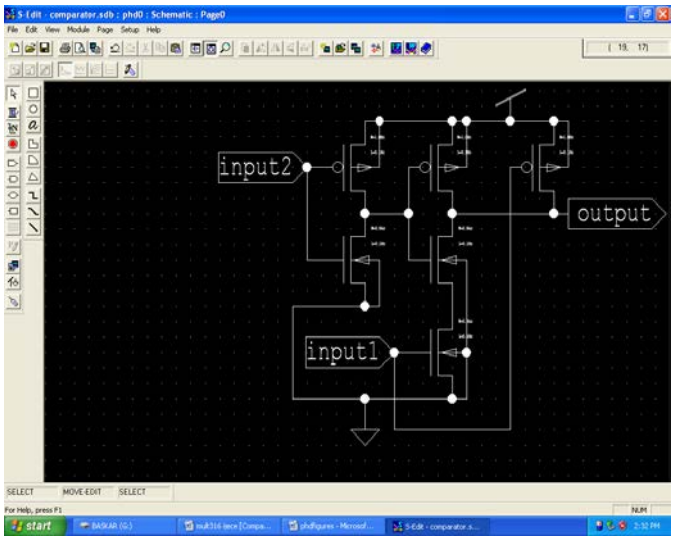

Fig 10: Step 5 complete circuit.

The approach which we have presented here can be extendable to N-bit it's like with N inputs we will be having combinations's high's and Low's and if requirement is like I1,I3, I4,I6,I7 are High's and I2,I5,I8(IN) are Low's then all the High corresponding inputs are NMOS Transistors in series but whether in the First Demarcation line or in the Second Demarcation line depends on Output High(Low) requirement, all the Low corresponding inputs are PMOS Transistors in series but whether in the First Demarcation line or in the Second Demarcation line depends on Output Low(High) requirement,

3. Adder

We have designed Adder by taking the general block diagram of PASTA [10] in which it has blocks like MUX, Half-Adder and Completion Detection Unit. MUX has been designed by using Static CMOS, Half-Adder sum part designed by using Transmission gate based CMOS and carry part by Static CMOS, and Completion Detection Unit by using Dynamic logic.

We have developed our own blocks named mymux, XOR and Completion Detection Unit, all these were designed by using Static CMOS. MUX in PASTA [10] can be replaced with mymux, Half-Adder in PASTA[10] can be replaced with myXOR and Completion Detection Unit is the same but designed with Static CMOS.

Mymux block is just the complemented output of MUX, MyXOR block has two outputs, in general XOR gate has only one output but the XOR which we have designed has two outputs and it is like utilizing efficiently Demarcation lines and our block has two Demarcation lines one has function of NOR other has function of XOR. Since mymux block is designed in a complemented manner, NOR gate can implement required function. Completion Detection Unit has very high fan-in it is nearly N+1 where N is total number of bits. To avoid speed degradation buffers can be introduced and requirement of how many buffers is directly proportional to N. Even though this approach needs to sacrifice Area it is mandatory.

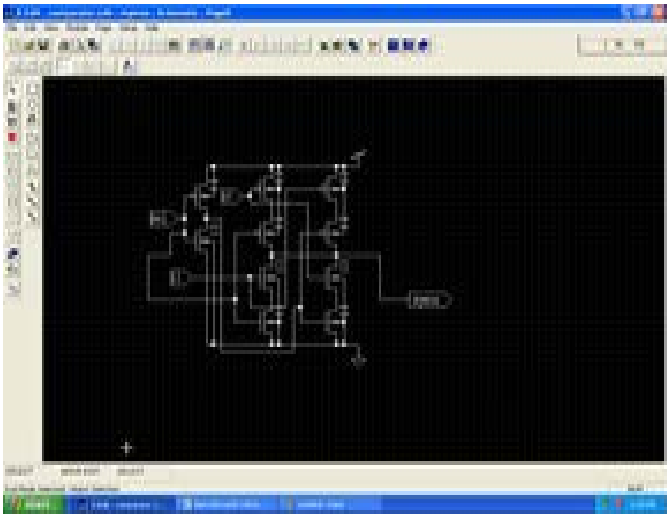

Fig 11: Proposed Multiplexer

Proposed mux has 10 number of Transistors and when sel='0' then complement of I0 will be selected and when sel='1'then complement of I1 will be selected.

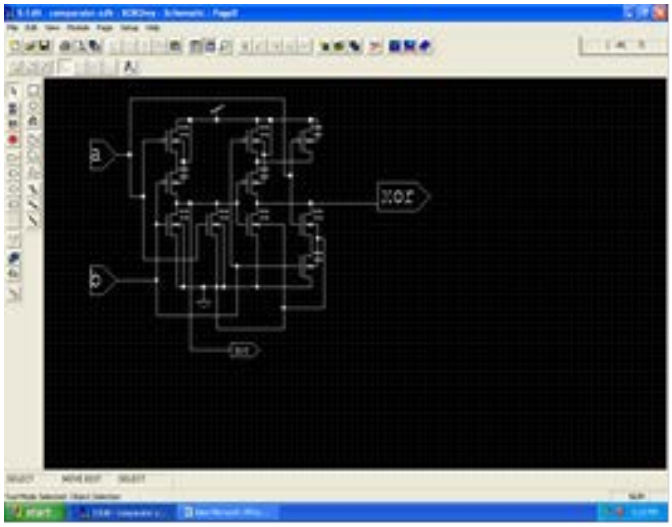

Fig 12: Two input – Two output XOR block

XOR block has 10 number of transistors and it has two outputs first Demarcation line has nor function and second Demarcation line has xor function, it has two sub-circuits in it one is nor is circuit other AOI 21

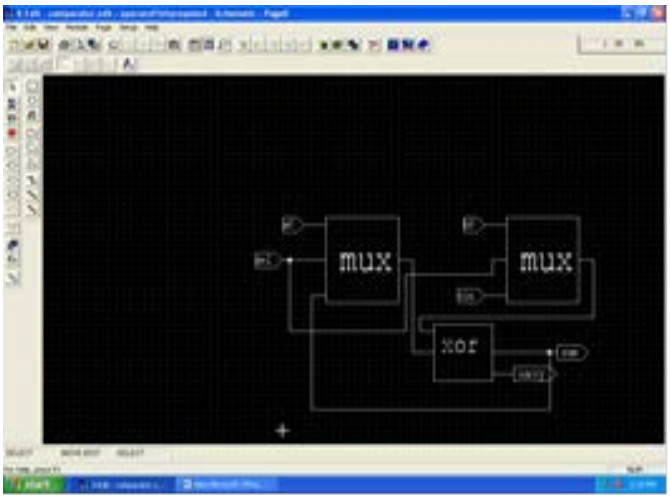

Fig 13: proposed 1-bit operand block

1-bit operand block has two 2 to 1 MUX and one XOR, and XOR second output is carry and sum output is fed back to the MUX.

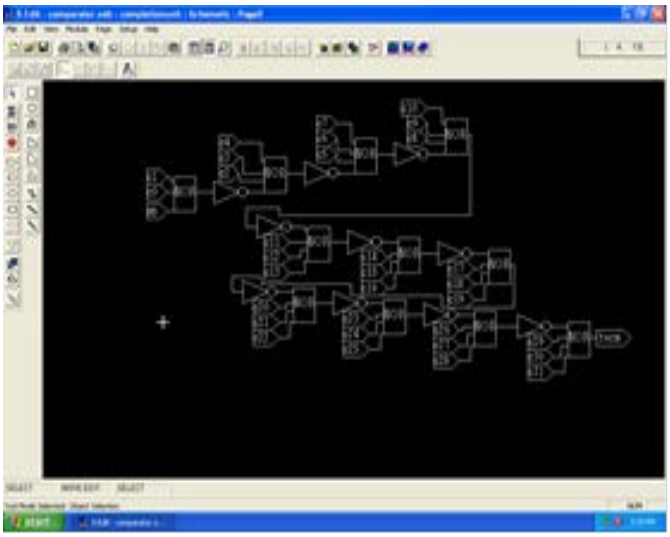

Fig 14: proposed Completion Detection Unit

Completion Detection Unit has one 3-input nor gate which requires 6 Transistors, ten not gates which requires 20 Transistors and ten 4-input nor gate which requires 80 Transistors leading to a total of 106 Transistors. Here fan-in is very much limited even though transistor count is increased for sure speed will be enhanced.

4 Static Cmos

The main advantage of Static CMOS is Robustness, low power consumption as well as Full output voltage swing if P-MOSFET is ON condition then N-MOSFET is OFF. More number of transistors required for Static CMOS, we require T-number of transistors in the PULL-DOWN network. WHILE, in Static CMOS network T-number of transistors in pull up network ARE PRESENT. The full voltage levels can make sure in the upcoming section's N-MOSFET'S and P-MOSFET'S fully on or off AS STATIC CMOS has advantage of full output voltage swing. If the output is Logic '1' and Logic '0' or vice versa the circuit can be designed. the differentiation between output voltage high logic level and output voltage low logic level is easy and this will be even more beneficial when the technology is scaled down, the Logic '1' range and Logic '0' range will come down when the supply voltage is less. Even while it is recommended that not more than 4 number of transistors should be in series in PULL-UP or not more than 6 Transistors should be in series in PULL-DOWN region as delay is going to be worse, variation is because NMOS is faster than PMOS. Our Design has only 4 number of maximum Transistors in series of pull-up and 2 in number of pull-down.

5. Performance Analysis

Design of Adder which can be extendable upto N-bit are done by using STATIC CMOS logic style. AREA comparison of Mux shown in table 1 in which 2 transistors were reduced. AREA comparison of Half-Adder in which 6 transistors were reduced are shown in table 2. AREA comparison of 1-bit operand in which 10 transistors were reduced is shown in table 3. Table4 shows AREA comparison of N-bit operand in which N*10 transistors were reduced are shown in table 4. AREA comparison of 32-bit Adder in which 248 transistors were reduced are shown In table 5. Table6 shows AREA comparison of 32-bit completion detection unit in which 72 transistors were increased due to Static CMOS technology which by default takes less number of transistors and we have also further added many buffers to increase the speed.

Table 1: Comparision Report For Area Of Mux 2 To 1

TOTAL	Design in Reference1	Proposed Design (Static cmos)
Area(number of transistors)	12	10

Table 2: Comparision Report For Half Adder

TOTAL	Design in Reference1	Proposed Design (Static cmos)
Area(number of transistors)	16	10

Table 3: Comparision Report For 1-Bit Operand

TOTAL	Design in Reference1	Proposed Design (Static cmos)
Area(number of transistors)	40	30

Table 4: Comparision Of Area In Two Designs For N-Bit Operand

TOTAL	Design in Reference1	Proposed Design (Static cmos)
Area(number of transistors)	N*40	N*30

Table 5: Comparision Report For 32-Bit Adder

TOTAL	Design in Reference1	Proposed Design (Static cmos)
Area(number of transistors)	(32*40)+(32+2) =1314	(32*30)+106 =1066

Table 6: Comparision Of Area In Two Designs For 32-Bit Completion Detection Unit

TOTAL	Design in Reference1	Proposed Design (Static cmos)
Area(number of transistors)	34	106

Table 7: Comparision Of Power In Two Designs For Mux

	Design in Reference1	Proposed Design (Static cmos)
Average Power Consumption	8.746993e-010 watts	6.511302e-010 watts

Table 8: Comparision Of Power In Two Designs For Half-Adder(Xor)

	Design in Reference1	Proposed Design (Static cmos)
Average Power Consumption	8.847008e-010 watts	7.058207e-010 watts

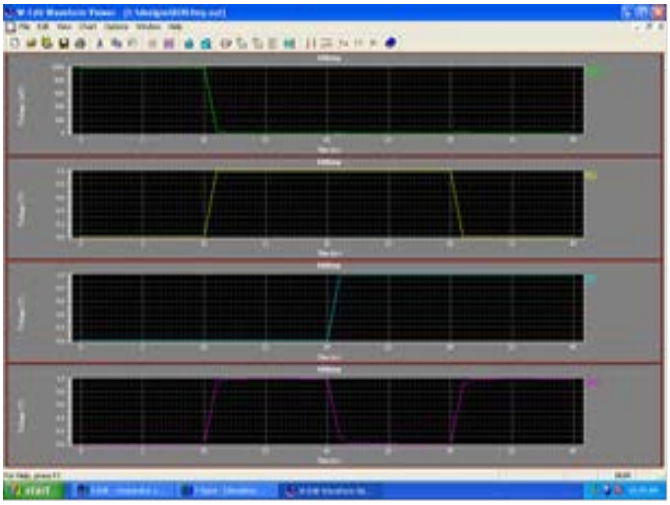

Fig 15: Simulation Result of Two input – Two output XOR block

Here Carry output has a function of NOR because in the earlier stage itself Multiplexer output is designed in the Complemented manner

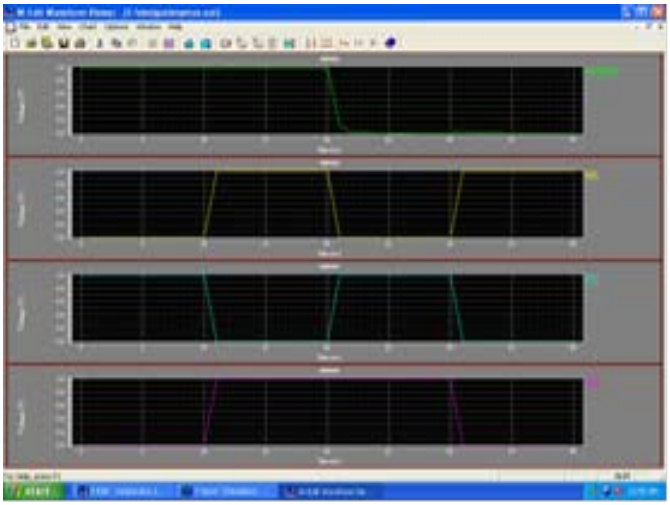

Fig 16: Simulation Result of proposed Mux

When selection line is equal to ’0’ or ‘1’ then Complemented version of the corresponding input will be the output

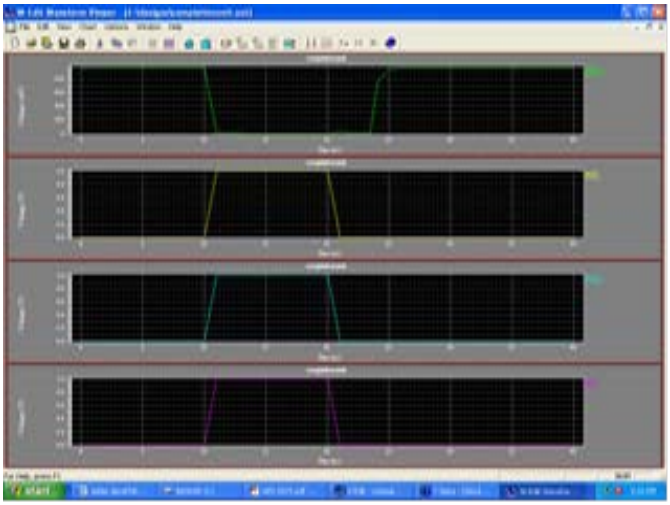

Fig 17: Simulation Result of proposed Completion detection unit

We were able to Design 32-bit unit by introducing many Buffers in the Circuit so Speed by Default will not be degraded and Area has been sacrificed to enhance the Speed and it does not have any problems of Dynamic circuits as in [1] where the Completion unit is being designed in Dynamic logic.

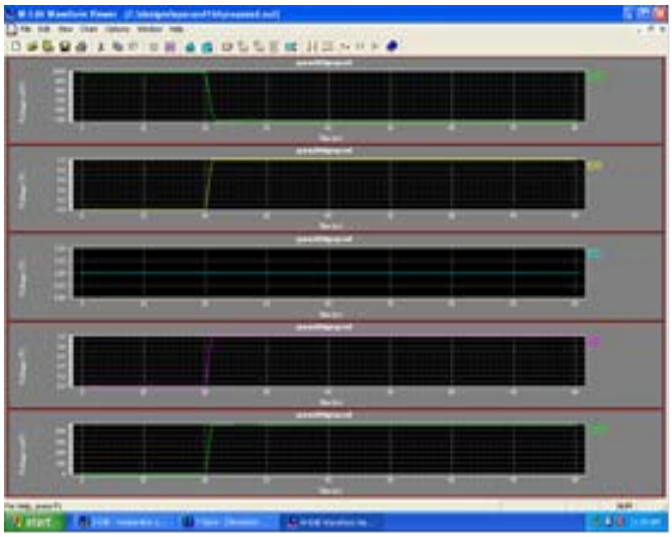

Fig 18: Simulation Result of proposed 1-bit operand unit when in operand reading mode operands will be read then next feedback (Carry) path will be active and in which Carry output has 550 milli volts.

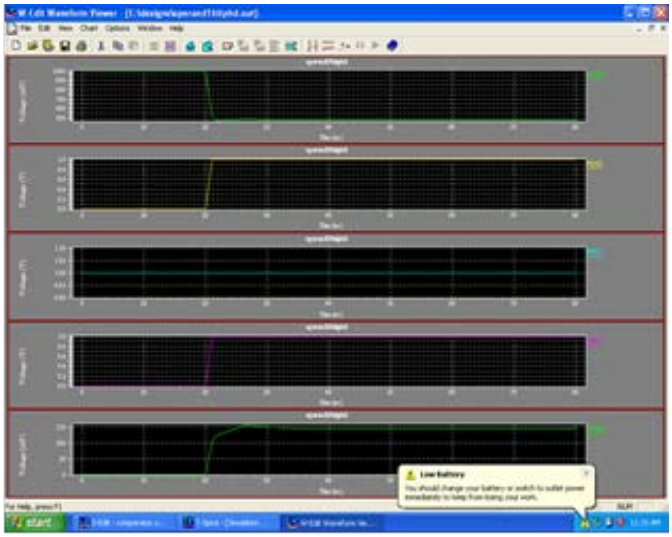

Fig 19: Simulation Result of 1-bit operand unit

Above result indicates that in feedback (Carry) path Carry output has only 150 milli volts. Power comparison reveals that cells which were being replaced has less power consumption. Since all the cells in our design based on Static CMOS, Layout optimization is also possible. One of the cells which are used in [1] are based on Dynamic logic which has charge sharing problems as well as more noise, another cell used Transmission Gates in there will be no power rails.

Conclusion

As area is proportional to Cost it has been a major constraint. Today Power and speed also started gaining more importance. our idea with the help of full custom design allows us to make our own circuit by taking the leaf level cells as gates or Transistors. Since, our Design is implemented in Transistors we have been able to optimize area and power constraints. Though we want Speed to be more, which is possible because of optimizing the logic, we haven't sacrificed on any Design constraint. We have designed our Adder by using STATIC CMOS logic that generally requires more number of transistors. While we are able to design the same by using less number of transistors. By following our approach we can achieve huge reduction in Transistor count, in spite of following the Architecture of PASTA, we have redesigned the blocks.

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