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Design and simulation of low area and low delay modified 32-BIT SQRT carry select adder

[1] CH. Sandeep, [2] Dr. GV Sridhar

[1] PG Student, Dept. of ECE, Avanthi College, Tagarapuvalasa, Andhra Pradesh, India
[2] Professor, Dept. of ECE, Avanthi College, Tagarapuvalasa, Andhra Pradesh, India

Abstract
In present scenario vlsi plays a major role in many analog and digital circuits the performance of the processor has became high power, low speed and high area so overcome these parameters the multipliers and adders plays a crucial role in many digital signal processors In the present approach carry select adder (CSLA) is one of the fast adder used in many digital signal processing applications as well as ALU when compare to carry look ahead adder the CSLA occupies low area and high speed. From the structure of the CSLA, there is scope for reducing the area and delay in the CSLA. The thesis uses a simple and efficient gate-level modification to significantly reduce the area. In the present paper modified 32 bit SQRT CSLA is compared with the 32-bit conventional SQRT CSLA architecture.
In the present paper the modification is done using binary to excess code converter technique (BEC-1) by replacing with the RCA stage of conventional method of 32 bit CSLA. The design is checked synthesized and simulated on Xilinx ISE design suite 14.1. The area comparison is done in respect of LUTs. Proposed design has reduced area and delay as compared with the conventional SQRT CSLA with only a slight increase in the delay. The thesis evaluates the performance of the design in terms of area and delay. The result shows that the modified SQRT CSLA structure as performed low area and low delay when compared to conventional SQRT CSLA.

Keywords: SQRT CSLA, Modified CSLA, BEC-1, RCA, XILINX ISE Design Suite 12.1, Verilog VLSI

Introduction
In high speed vlsi circuits to propagate a carry through the adder and the speed of addition is limited by the time required. The Design of low area and high-speed are one of the most important areas of research in VLSI system design. In an adder the sum for each bit position is generated serially only after the previous bit position has been summed and a carry propagated into the next position.To avoid the problem of carry propagation delay the CSLA is used in many computational systems independently generating multiple carries and then select a carry to generate the sum. However, the CSLA as low area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input LOW(Cin=0) and Cin=HIGH then the final sum and carry are selected by the multiplexers. The main purpose of this paper is Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and delay.

2. Basic Adder Block
The Basic adder block is a Ripple carry adder, Mux and BEC is explained in this section. In this paper the theoretical approach as been calculated and and show how the delay and area effect the total implementation. The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. In an adder the number of gates in the longest path of a logic block that contributes to the maximum delay. The low area and low delay is done by counting the total number of AOI gates required for each logic block. Based on this technique, the blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table 1.

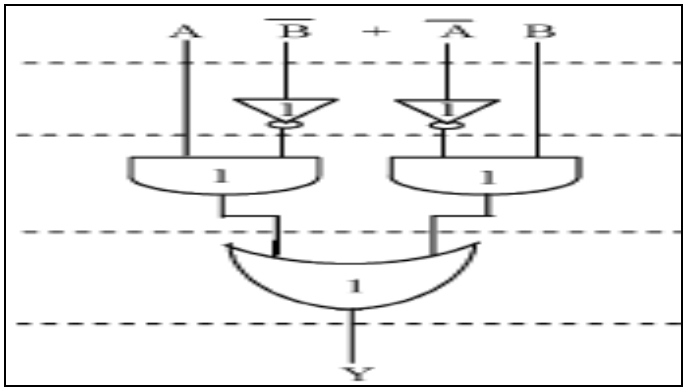

Fig 1: Delay and Area evaluation of an XOR gate.

Table 1: Delay and Area Evaluation of CSLA

Adder Blocks	Delay	Area
XOR	3	5
2:1 MUX	3	4
Half Adder	3	6
Full Adder	6	13

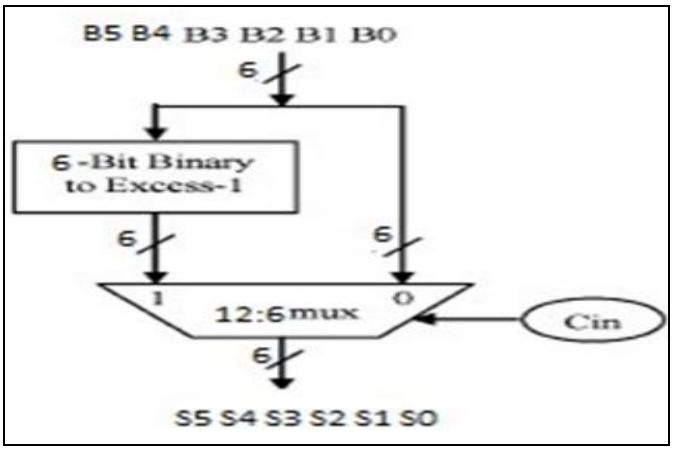

Fig 2: 4-bit BEC with 8:4 mux

ALU operations like multiplication, division, addition, subtraction, are the basic operations to be implemented in digital computers using basic gates like AND, OR, NOR, NAND etc. are the basic operations to design any vlsi circuit in all the ALU operations we can implement addition then it is easy to perform multiplication, subtraction or division. Two one bit binary numbers can be added by using Half Adders. The main purpose of the full adder is to add n-bit binary numbers to create a logical circuit using multiple full adders. Each full adder inputs Cin which is the Cout of the previous adder. This kind of adder is a Ripple Carry Adder, since each carry bit "ripples" to the next full adder. The first full adder may be replaced by a half adder. The block diagram of 32-bit Ripple Carry Adder is shown here below

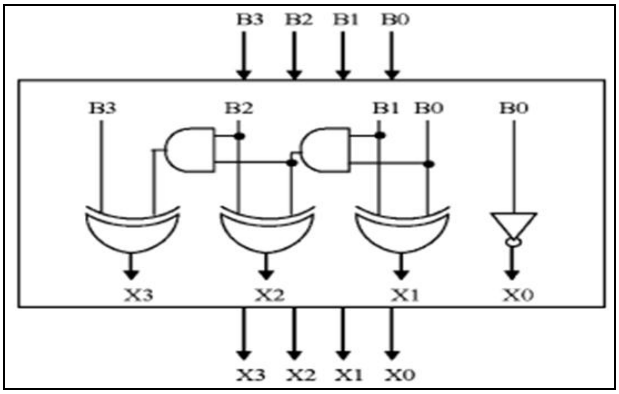

Fig 3: 4-bit BEC

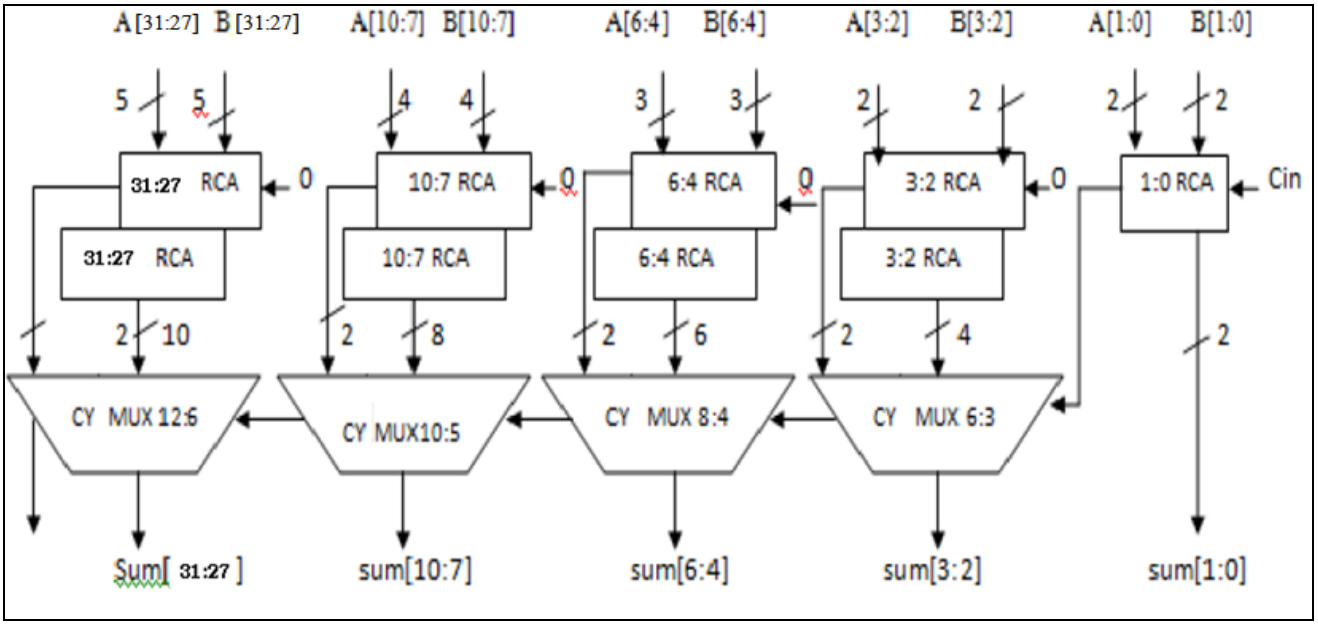

Fig 4: 32-bit SQRT CSLA using RCA

The ripple carry adder as its own structure which useful to design any high speed vlsi circuit, however the ripple carry will perform very slow speed when compared to cla due to delay using more number of full adder circuits, the carry bit to be calculated from the previous full adder since each full adder must wait for low delay. By observing the full adder circuit the delay can be calculated. The below full adder circuit requires three levels of logic. In a 32-bit [ripple carry] adder, there are 32 full adders, so the critical path (worst case) delay is 31 * 2(for carry propagation) + 6(for sum) = 68 gate delays However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input low (Cin=0) and high (Cin=1) then the final sum and carry are selected by the multiplexers The structure of the 32-bit SQRT CSLA using RCA is shown in Fig. The circuit has five groups of different size RCA. The RCA has low area and low delay evaluation from which each group are shown in Fig. in which the numerals within specify the delay values, e.g., sum2 requires 10 gate delays. The steps to the evaluation are as\ follows. 1) The group2 has two sets of 2-bit RCA. Based on the consideration of delay values of the arrival time of selection input of 6:3 mux is earlier than and later than. Thus, is summation of and 2) Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the RCA's. Thus, the delay of group3 to group5 is determined, respectively as follows: 3) The one set of 2-bit RCA in group2 has 2 FA and the other set has 1 FA and 1 HA coming to low area count, the total number of gate counts in group2 is determined. For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

3. Carry select adder using BEC-1

The structure looks like a regular 32-bit SQRT CSLA, in the modified circuit the only change is that, we replace RCA with Cin=1 among the two available RCAs in a group with a BEC. The binary to excess code convertor (BEC) can perform the operation is similar to that of RCA, that means RCA block can be replaced with BEC-1 with Cin=1.The Figure shows the modified diagram of 32-bit SQRT CSLA. The binary to excess code BEC-1 it as logic 1 bit more than the RCA bits. The diagram of modified block can be divided into various groups of variable sizes of bits with each group having the ripple carry adders, BEC and mux 1st group contain one RCA which is having input of lower significant bit and carry in bit and produces result of sum (1:0) and carry out which is acting as mux selection line for the next group. The Modified CSLA is replaced with the optimized XOR gate in AOI of Modified Area Efficient CSLA with BEC there is reduction of gates by replacing n bit RCA with n+1 bit BEC. The optimization can be done by replaced with XOR gate is used in Modified CSLA, the verification shows the large reduction in number of gates, For selection pupose MUX is used either the BEC output or the inputs given directly to a BEC circuit. In this design, the major function of MUX is to derive the adder speed.

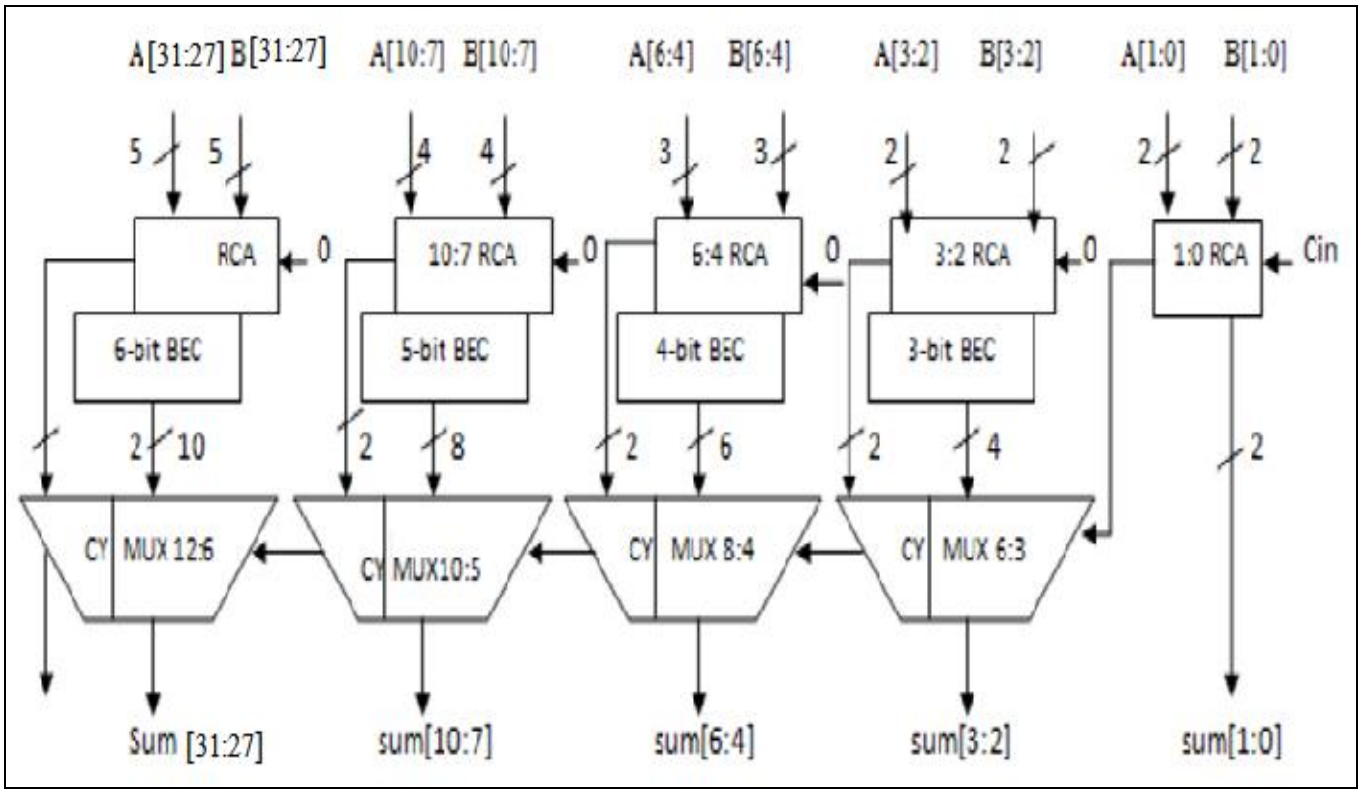

Fig 5: Structure of 32-bit modified SQRT CSLA Using BEC-1

Table 2: delay and area count of 32 bit SQRT CSLA

S. No	Parameter	SQRT CSLA Using RCA	SQRT CSLA Using BEC
1	Area	42	46
2	Delay(ns)	16.26	14.66

Table 3: Comparision in terms of area and delay

Group	Area	Delay
Group2	43	13
Group 3	61	16
Group4	84	19
Group5	107	22

4. Delay, area evaluation methodology of regular CSLA with modified CSLA

Delay and area evolution of regular CSLA with modified CSLA is shown in below table. In regular CSLA the area is reduced as compared to modified CSLA. Delay is reduced by using modified SQRT CSLA RCA as compared to regular SQRT CSLA BEC-1. The Low area comparision shows that the number of LUT will be increased for modified method for the 32-bit SQRT CSLA.

5. Results

The implemented Design in this paper has been simulated using VERILOG. The 32-bit adder are designed and simulated using VERILOG and the results are compared. After simulation the different size codes are synthesized using Xilinx ISE 14.1, simulated files are imported into the synthesized tool and values of delay and area are noted.

6. Simulation Results

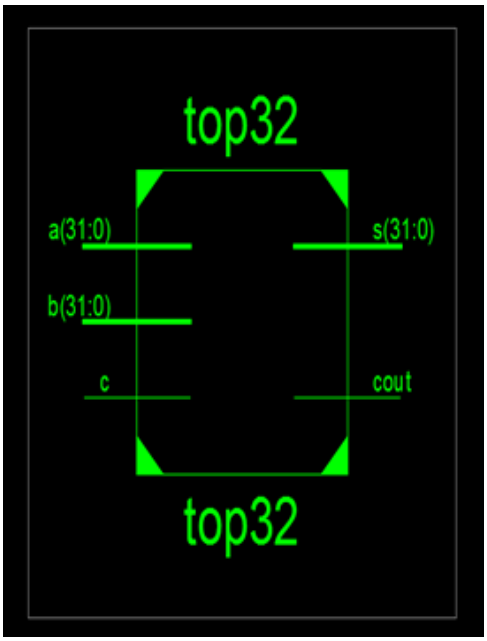

Fig 6: SQRT CLA 32-bit Top Module

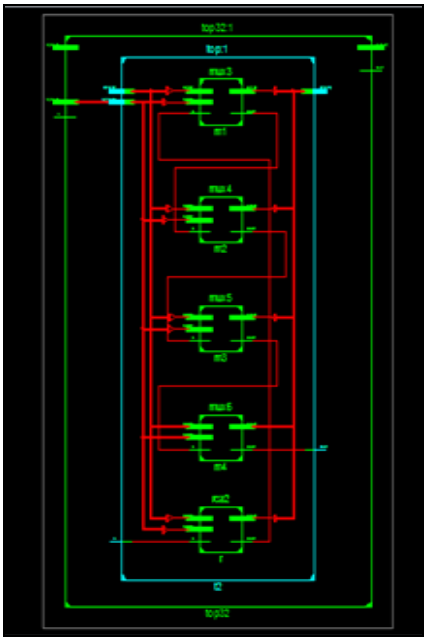

Fig 7: RTL schematic

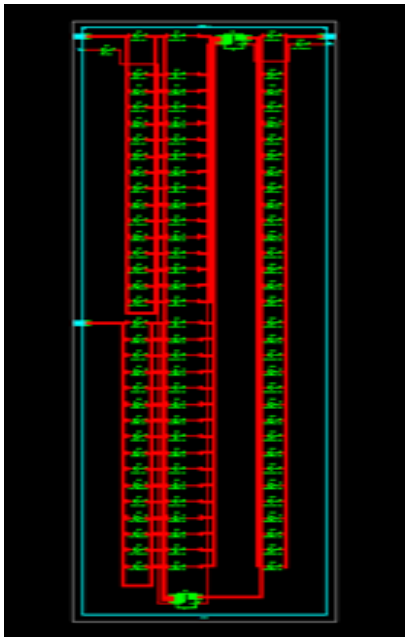

Fig 8: Technology schematic

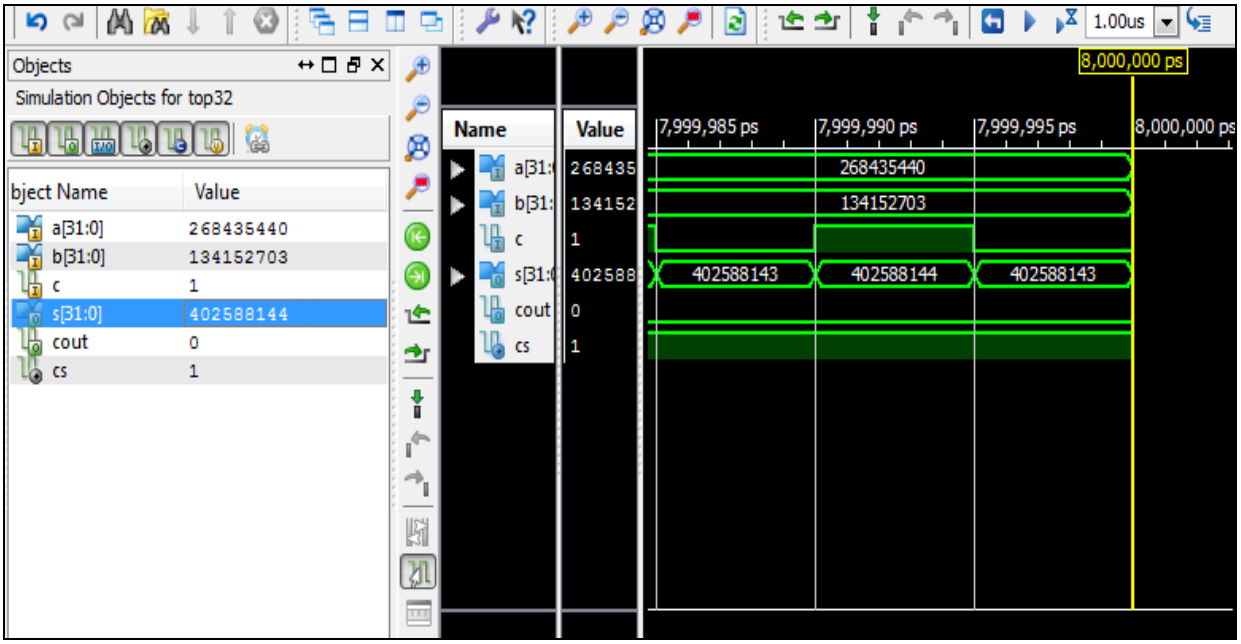

Fig 9: Simulation result of modified SQRT CSLA

7. Conclusion

In this paper the designing as well as implementation can be done for low delay and low area using a simple approach to reduce area and delay of SQRT CSLA using BEC architecture. The RCA with BEC in the structure is a great advantage to reduction in the number of gates. The result as shown in comparision table states that the modified SQRT CSLA has a slightly large area when compared with SQRT CLA BEC for low order bit as well as r higher order bit and also delay is reduced to a great extent. Thus the result shows that using modified method the area and delay will decrease so it is a good alternative vlsi technique for high speed constraint devices

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