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Performance analysis of an efficient reversible design of BCD adder

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Abstract
At Present the vlsi plays a major role for low power constraints devices like processors in the processing unit multipliers and adders makes a crucial role not only for low power but also low area and low delay in the present paper reversible logic gates are used for reversible operation The important reversible gates like Faynman Gate, Fredkin gate, toffoli gate, MTSG gate, CNOT gate and peres gate etc with the help of normal logic gates the complexity of the gate delay can be increased and power will be more so to over come these parameters in this paper the 4bit BCD can be designed the reversible operation can be applied so the low power can be obtained as well as delay the comparison shows the how much power is consumed by using reversible logic design the simulation and synthesis can be obtained using Xilinx tool.

Keywords: Low-power VLSI, Low-power CMOS design, reversible logic, quantum cost, reversible counters

Introduction

Recently due to its ability to reduce the power dissipation, reversible logic has received a great attention.as it is the main criteria in low power vlsi design.in low power cmos ,optical information proccessin ,DNA computing, quantum computation as well as nanotechnology this logic has wide number of applications because of information loss, irreversible hardware computation would result in energy dissipation.as per the research by landauer's, the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules, where K=1.3806505*10-23m2kg-2K-1 (joule/Kelvin-1) is the Boltzmann's constant and T is the temperature at which operation is performed [1]. Usually the heat generated as a result of the loss of one bit of information is very less at room temperature. while, in case of high speed computational works where the number of bits are more, the heat dissipated by them will be quite large so as to effect the performance and results in reducing the lifetime of the components. Back in 1973,as Bennett showed that KTln2 energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs [2] .the advantage of reversible logic to be able to support the process to run the system in both forward and backward proves that reversible computations can generate inputs from outputs and can return back to any point of the computation history. A reversible circuit is when the input vector can be uniquely recovered from the output vector and also when there is a one-one correspondence between the input and output assignments. which specifies that not only the outputs are uniquely determined from the inputs, but inputs can be recovered from outputs as well. hence, energy dissipation can be eliminated if the computation is of no loss.

The Concept

In present Reversible logic is a method for constructing computers that produce no power dissipation [1]. The logic operation can be done by Reversibility this approach is having many applications like computing as well as DSP applications. Specifically, the basic fundamentals of reversible computing are depend on the entropy, heat transfer between molecules in a system, the probability of a quantum particle can be replaced by a particular state at any given time, and the quantum electrodynamics between electrons when they are in close proximity.

Motivation behind reversible logic

The main principle of reversible computing is that a bijective device which shows an identical number of input and output lines will produce a computing environment where the electrodynamics system allow for prediction of all states but not only future states it also depends on present state, resulting in no heat dissipation [2] A circuit is reversible when there is a one-to-one mapping between sets of input and output values. The input states can be always reconstructed from the values of output states. Bennett's [3] theorem suggests that binary technology will be used for kind of a reversible gates in order to lower the power dissipation. The reversible operation can depends upon quantum dots and DNA circuit realization technologies Generally we use irreversible logic for VLSI System and implementations. The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit. The advantages of reversible logic circuits are low cost, delay, number of gates used. It has voluminous applications in quantum computing, optical computing, quantum dot cellular automata and digital signal processing. Reversible Gates are efficient than the conventional Logic gates [4] Power dissipation is one of the most important factors in VLSI circuit design.

Reversible logic gates

The reversible logic gates as following design constraints

- It do not allow fan-outs.
- It should have minimum quantum cost.

- The circuit as minimum number of garbage outputs.
- The reversible logic circuits must use minimum number of constant inputs.
- The reversible logic circuits must use a minimum Logic depth

Reversible logic gates

i) Feynman Gate

Feynman gate is a 2*2 one through reversible gate as shown in figure 1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A xor B. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

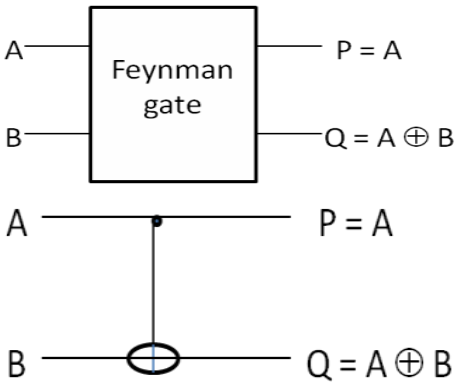

Fig 1: Feynman Gate

Table 1: Truth table of Feynman gates

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

ii) Toffoli Gate

In the logic circuits, the Toffoli gate (also CCNOT gate) invented by Tommaso Toffoli, is a universal reversible logic gate, which defines that any reversible operation can be constructed from Toffoli gates. It is also known as the "Controlled-Controlled-Not" gate, which describes its action. It has 3-bit inputs and outputs; if the first two bits are set, it inverts the third bit, otherwise all bits stay the same.

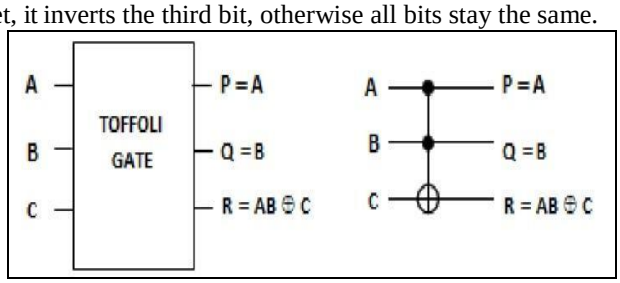

Fig 2: Toffoli gate

Table 2: Truth table of Toffoli gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

iii) Fredkin Gate

The Fredkin gate (also CSWAP gate) is a computational circuit suitable for the reversible computing, invented by Ed Fredkin. It is universal, which means that any logical or arithmetic operation can be constructed entirely of Fredkin gates. The Fredkin gate is the three-bit gate that swaps the last two bits if the first bit is 1.

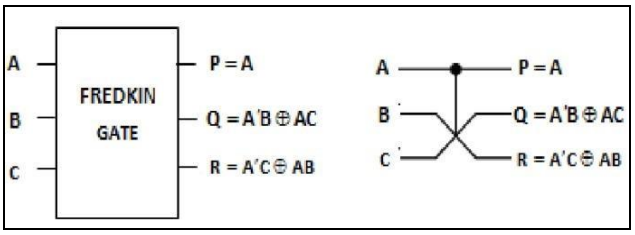

Fig 3: Fredkin gate

Table 3: Truth table of fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

iv) Peres Gate

Peres gate is a 3*3 reversible gate. It is also known as New Toffoli gate. It is constricted from CNOT Gate and TOFFOLI gate. The Peres Gate can acts as a Half Adder

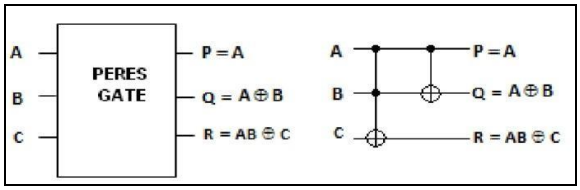

Fig 4: Peres Gate

Table 4: Truth table of peres gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

v) CNOT Gate

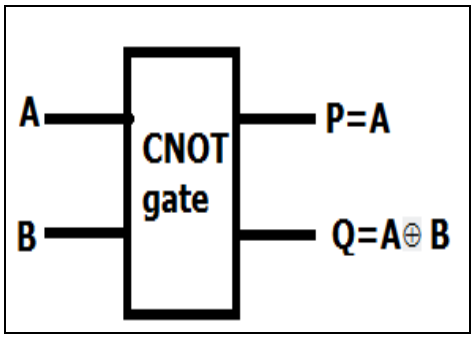

Fig 5: CNOT GATE

Table 5: Truth Table CNOT GATE

Inputs		Outputs	
A	**B**	**P**	**Q**
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

In computing science, the controlled NOT gate (also C-NOT or CNOT) is a quantum gate that is a most important component in the construction of a quantum computer. Any quantum circuit can be simulated to an arbitrary degree of accuracy using a combination of CNOT gates and single quantum bit rotations. The CNOT gate is the "quantization" of a classical gate.

vi) MTSG Gate

MTSG Gate is a 4*4 reversible logic gate. It is constricted from cascading of two Peres gate by providing 0 in the input C; this gate can easily realize the classical full adder. For designing n-bit binary ripple carry adder, n MTSG gates are required.

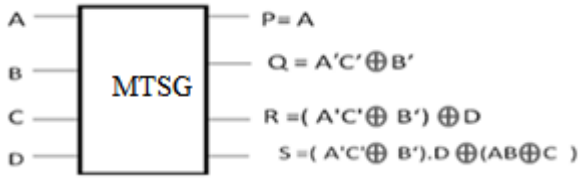

Fig 6: MTSG GATE

Table 6: Truth table of MTSG gate

Inputs				Outputs			
A	**B**	**C**	**D**	**P**	**Q**	**R**	**S**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	0
1	1	1	1	1	0	1	0

Reversible BCD Adder consists of three basic components

- 4-bit Parallel Adder
- Overflow Detection Logic
- Overflow Correction Logic
- verflow Correction Logic

Here, one 4-bit parallel adder is used for the binary addition of the numbers, a combinational circuit is used for detection of BCD overflow and another 4-bit parallel adder is used for error correction if overflow occurs The general idea of these designs is as follows: In the first 4-bit parallel adder, initial sum is produced by the binary addition of the two BCD Adders.

From fig 6 in the detection unit, The overflow of BCD is detected. The most important parameter is fan-out is restricted in the reversible logic design From fig 6 in the correction part, a 4 bit parallel adder is used to add the error correction value, i.e. in binary 0110, if overflow occurs. Otherwise, output produced by the first 4-bit parallel adder becomes the final output. However, there are scopes to improve the designs in terms of number of gates, garbage outputs and delay. Design of a reversible Binary coded decimal adder is done overcoming the existing design. The block diagram of a proposed Reversible Binary Coded Decimal Adder as follows

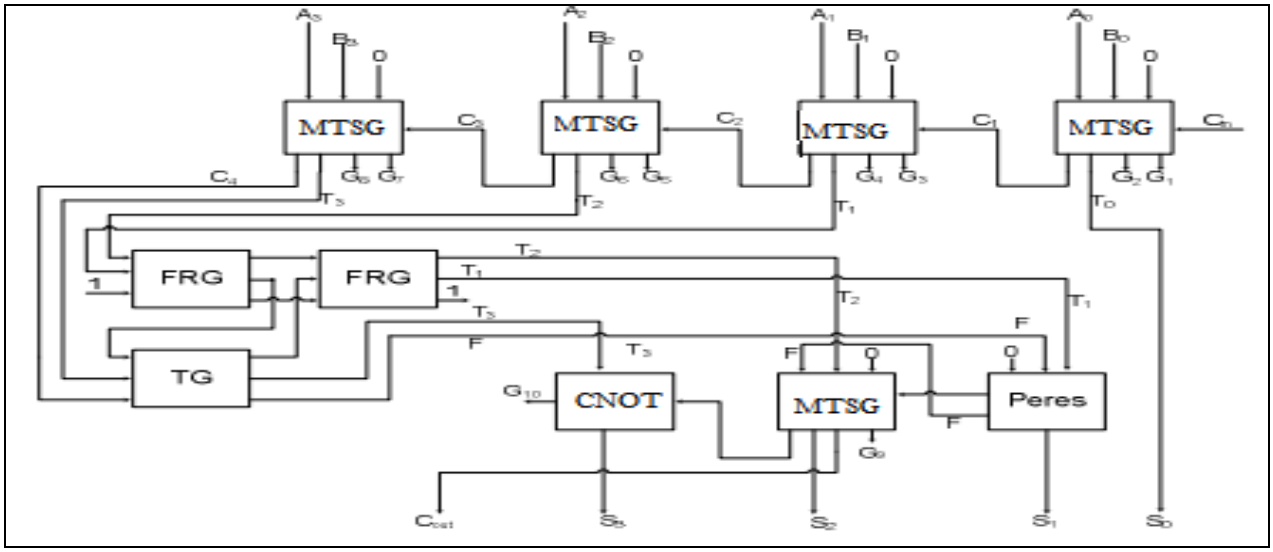

Fig 7: Block Diagram of Proposed 4-bit Reversible BCD Adder

Existing Design of Binary Coded Decimal Adder

The Existing Irreversible Design of a Binary Coded Decimal Adder consists of mainly three blocks namely:

- 4-bit Full Adder
- Detection Unit
- Correction Unit

The first part 4-bit binary adder is cascade of four full adders. Two AND gates and one OR gate is required for design the detection unit The third part correction unit adds 0 to the binary number if the binary result is less than10 and adds 6 to the binary result if it is more than 9.Binary full adder is a basic circuit for designing binary arithmetic units such as n-bit binary adder, sub tractor and multiplier. In the same manner, a BCD adder/subtract or is a basic circuit for designing BCD arithmetic units such as BCD n-bit adder/subtractor.

The block diagram of a 4-Bit Binary Coded Decimal Adder is shown below

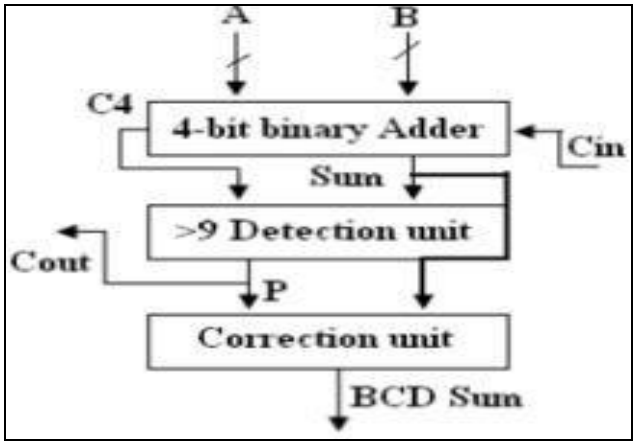

Fig 8: Block Diagram of Existing BCD Adder

The circuit diagram of the above circuit is shown below:

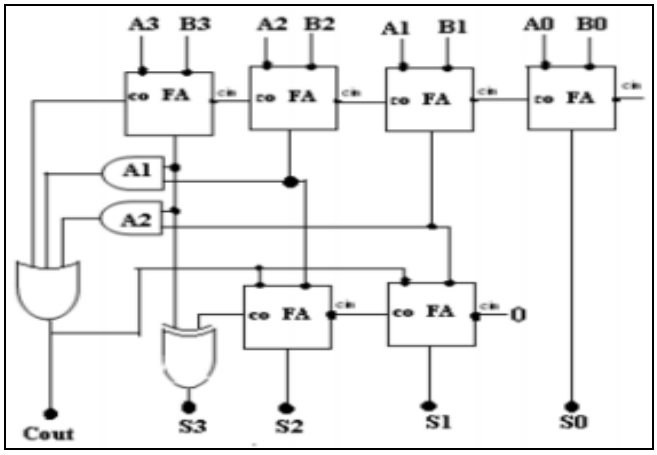

Fig 9: Circuit Diagram of Existing BCD Adder

Simulation Results

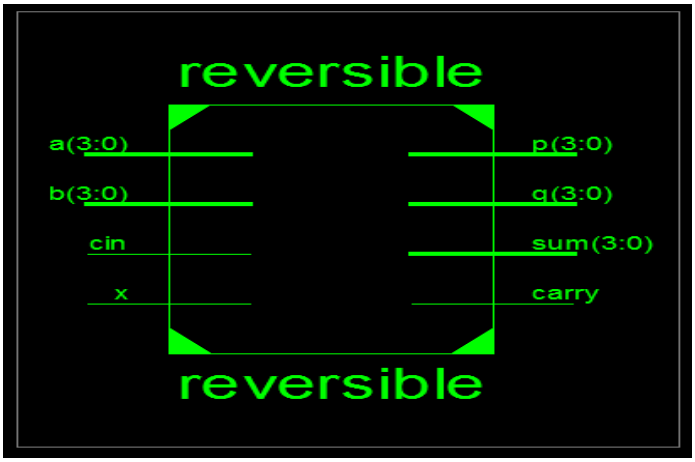

Fig 10: Pin diagram

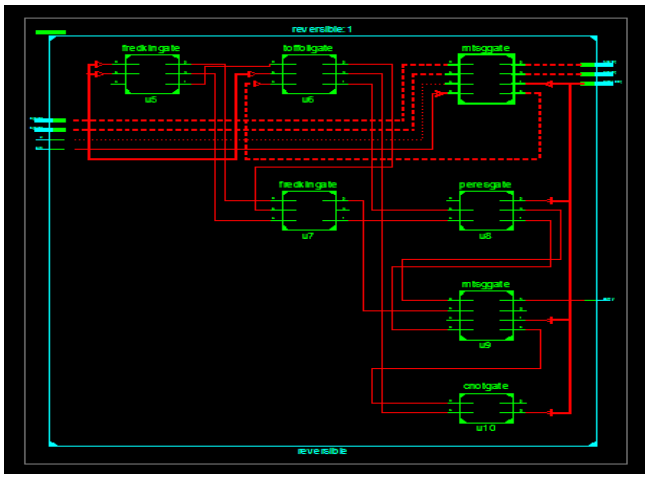

Fig 11: RTL schematic

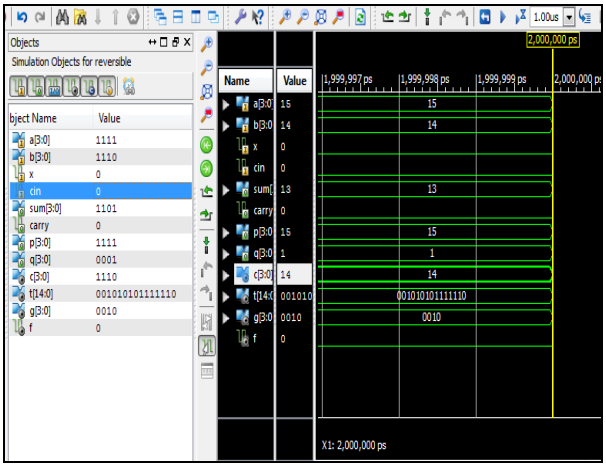

Fig 13: Simulation result of proposed BCD adder

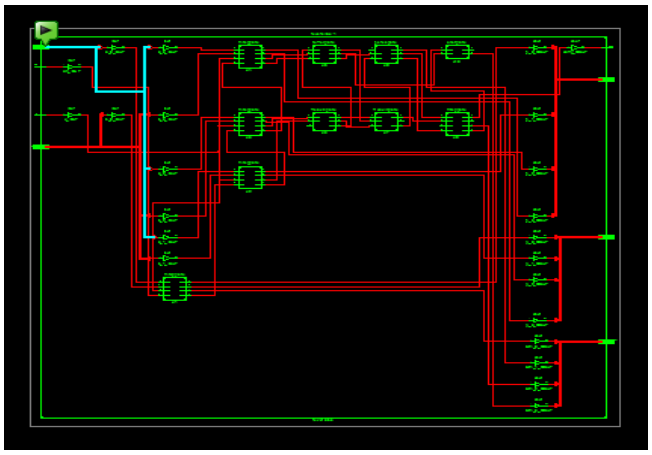

Fig 12: Technology schematic

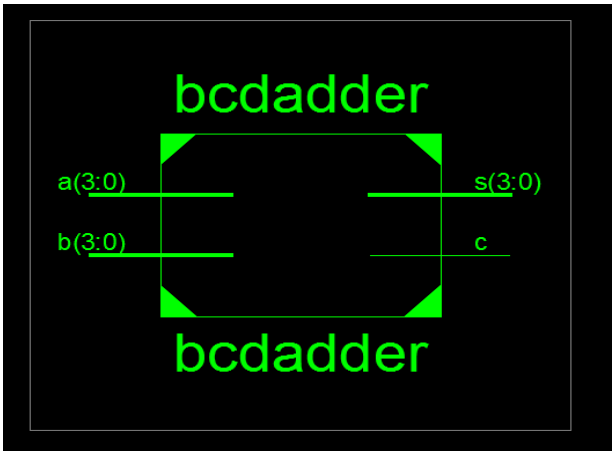

Fig 14: Pin diagram

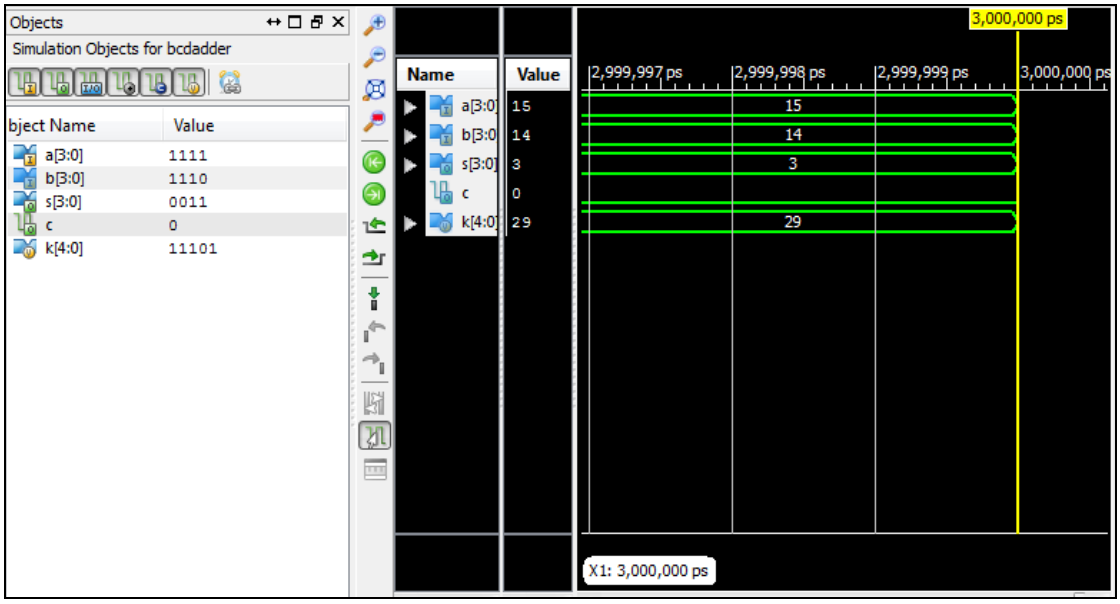

Fig 15: Simulation result of existing BCD adder

Conclusion

In the present approach the multipurpose binary reversible gates is to be realized. Such gates can be used in regular circuits realizing Boolean functions. In the same way it is possible to construct multiple-valued reversible gates having similar properties. The proposed asynchronous designs have the applications in digital circuits like a Timer/Counter, building reversible ALU, reversible processor etc. with the help of this concept we can design complex reversible sequential circuits.

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